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ARM Architecture Introduction: Cortex M0, Cortex M1, Cortex M3 \u0026  
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- ARM Debug Interface v5, Architecture Specification (ARM IHI 0031)

Note A Cortex-M0 implementation can include a Debug Access Port (DAP). This DAP is defined in v5.1 of the ARM Debug interface specification, or in the errata document to Issue A of the ARM Debug Interface v5 Architecture Specification.

- Application Binary Interface for the ARM Architecture (The Base Standard) (IHI0036 ...

## ~~Cortex M0 Technical Reference Manual~~

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- Ultra-low power, energy-efficient operation.
- Excellent code density.

~~Cortex M0+ Devices — ARM architecture~~

The ARM Cortex-M is a group of 32-bit RISC ARM processor cores

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licensed by Arm Holdings. These cores are optimized for low-cost and energy-efficient microcontrollers, which have been embedded in tens of billions of consumer devices. The cores consist of the Cortex-M0, Cortex-M0+, Cortex-M1, Cortex-M3, Cortex-M4, Cortex-M7, Cortex-M23, Cortex-M33, Cortex-M35P, Cortex-M55.

~~ARM Cortex M — Wikipedia~~

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